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Question Paper Code : 21185

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Fifth Semester

Electrical and Electronics Engineering

EC 1307 — DIGITAL SIGNAL PROCESSING

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulation 2008)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Classify the type of signals.
2. What are the limitations of Digital Signal Processing?
3. What are the errors generated by A/D process?
4. Distinguish between causal and non causal systems?
5. What is zero padding? Why is it needed?
6. What is static and dynamic system? Give examples.
7. List the different types of structures for realizing FIR systems?
8. List some of the finite word length effects in digital filters?
9. What are the two types of quantization employed in digital system?
10. Sketch the noise probability density functions for rounding?

PART B — ($5 \times 16 = 80$ marks)

11. (a) Find the response of the time invariant system with impulse response $h(n)=\{1, 2, 1, -1\}$ to an input signal $x(n) = \{1, 2, 3, 1\}$.

Or

(b) (i) Test $y(n) = 2x(n)–b\ x(n–l)$ system for linearity. (10)

(ii) What are energy and power signals? (6)

12. (a) Find the general solution of difference equation $y(n) = x(n) - 3y(n\text{-}1)$ with initial condition $y(-1)=0$ and input $x(n) = n^2 + n$.

Or

(b) (i) Compute the linear convolution of the sequence $x(n) = \{1, 1, 0, 1\}$. (10)

(ii) Find the Z- transform of a digital impulse. (6)

13. (a) State and prove the properties of DFT. Interrelate between Z-Transform and DFT.

Or

(b) Draw the 2-point radix -2 DIT-FFT butterfly structure for DFT. Also compute the FFT of the sequence $x(n) = \{1, 2, 3, 4, 4, 3, 2,1\}$ using decimation-in-frequency algorithm.

14. (a) Design a low pass FIR filter that approximates the following frequency response,

$$H(f) = \begin{cases} 1; & 0 \le f \le 1000Hz \\ 0; & elsewhere in the range \quad 0 \le f \le fs/2. \end{cases}$$

Or

(b) Design a first-order digital Butterworth high pass filter which is equivalent to an analog filter with cutoff frequency 1 KHz at a sampling rate of 10^4 sps. Use bilinear transformation.

15. (a) In the IIR system given below the products are rounded to 4-bits (including sign bit) $H(z) = 1/(1-0.35z^{-1})(1-0.62z^{-1})$. Find the output roundoff noise power in

(i) Direct form realization (8)

(ii) Cascade realization. (8)

Or

(b) With relevant diagrams explain the architecture and features of TMS320C54X signal processing chip?

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